ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 10, October 2014

Design of a Low Power Clock Multi Band Network for Supplying the Multi Clock Domain Networks

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ABSTRACT: when working with IC's most of the power will be consumed for making the IC in to active working state. This depends on the clock distribution networks. Because the clock signals have the high switching activity. Normally for a multi clock domain networks the power consumed by the clock signals is too high to lower this we generally use multiple PLL's, in this project we aim for developing a low power single clock multiband network which will supply for the multi clock domain network. This design is highly useful for communication applications. A low power clock model network is designed for LAN using pulse-swallow topology and the design is modelled using Verilog simulated using Model sim and implemented in Xilinx.

KEYWORDS: Clock signals, Buffers, Multi band networks, Counters, AC-TSPC

I. INTRODUCTION

In some Wireless LAN applications such as Hiper LAN IT and IEEE 802.11a/b/g., are leading standards for high data transmissions and standards like IEEE 802.15 are very useful for low rate data transmissions. The main demand in VLSI circuits are to have lower power, low cost, high integration in designing the circuits and circuits which are re-useable are very needed. Especially in designing he FPGA circuits we need better building block to construct the optimized circuits having better clock signals and low power consumption circuits. For that we need to design better networks to give the supply to multiple networks operating at multiple bands. And when designing that the main consideration is to have the as lower consumption as possible. Usually the frequency synthesizers are implemented by a phase-locked loop (PLL) , but it consumes lots of power given to the IC. The integrated synthesizers for WLAN applications at 5 GHz consume up to 25 m W in CMOS realizations, where the first- stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range.

The best frequency synthesizer at 5 GHz consumes 9.7 mWat supply, where its complete divider consumes power around 6mW, where the first- stage divider is implemented using the source-coupled logic (SCL) circuit which allows higher operating frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers. The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5 GHz.

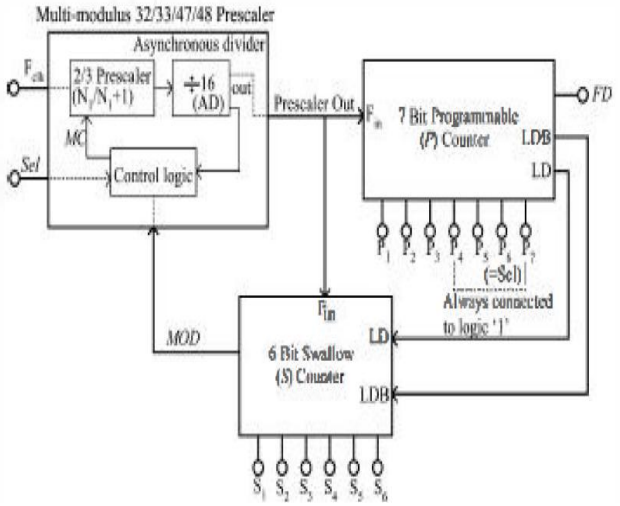

Figure [1] Proposed dynamic logic multiband flexible Divider.

The frequency synthesizer uses an E-TSPC pre-scaler as the first-stage divider, but the divider consumes around 6.25 mW. Most IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage while dynamic latches are not yet adopted for multiband synthesizers.

II. PROBLEM OVERVIEW

True single phase clock logic techniques, e.g. with alternating arranged N- and P-logic cells, yield easy to design circuits with standard cells and high speed potential. The disadvantages are a difficult clock tree design and high power consumption. To realize every logic function, dual rail or differential styles are chosen which increase clock load. We developed a method to speed up dynamic single clock circuits. The advantage of asynchronous logic is that the critical path delay is the sum

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International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 10, October 2014

of only the evaluation times of the single logic blocks without wasting time for waiting, latches, or redundant logic. Therefore, we assemble small asynchronous chains of dynamic logic blocks into one period of the global clock to minimize the unused time per clock cycle (AC-TSPC). However, the synchronous single phase clocking scheme is maintained. The advantages of this method are shorter latencies for calculations, power reduction by smaller clock trees and no need for latches, and a simpler clock distribution network due to increased clock skew tolerance. The results of the simulations of an 8x8 bit multiplier in TSPC and in AC-TSPC show an enhancement in power-reduction of 40% for the logic and of 89% for the clock tree with a latency reduction of 40% and more in comparison with TSPC. To overcome this problem with clock I am proposing a multi-modulus pre-scaler which is useful for the different applications.

III. EXISTING SYSTEM

In the two-phase clocking schemes described above, care must be taken in routing the two lock signals to ensure that overlap is minimized. While the C^2MOS provides a skew-tolerant solution, it is possible to design registers that only use a single phase clock. The True Single-Phase Clocked Register (TSPCR) proposed by Yuan and Svensson uses a single clock (without an inverse clock) [Yuan89]. The basic single-phase positive and negative latches are shown in Figure [2]. For the positive latch, when CLK is high, the latch is in the transparent mode and corresponds to two cascaded inverters; the latch is non-inverting, and propagates the input to the output. On the other hand, when CLK = 0, both inverters are disabled, and the latch is in hold-mode. Only the pull-up networks are still active, while the pull-down circuits are deactivated. As a result of the dual-stage approach, no signal can ever propagate from the input of the latch to the output in this mode. A register can be constructed by cascading positive and negative latches. The clock load is similar to A conventional transmission gate register, or C^2MOS register. The main advantage is these of a single clock phase.

The disadvantage is the slight increase in the number of transistors— 12 transistors are required. TSPC offers an additional advantage: the possibility of embedding logic functionality into the latches. This reduces the delay overhead associated with the latches. Figure [2] outlines the basic approach for embedding logic, while Figure 2(A) shows an example of a positive latch that implements the AND of In1 and In2 in addition to performing the latching function. While the set-up time of this latch has increased over the one shown in Figure 2(B), the overall performance of the digital circuit (that is, the clock period of a sequential circuit) has improved: the increase in set-up time is typically smaller than the delay of an AND gate. This approach of embedding logic into latches has been used extensively in the design of the EV4 DEC Alpha microprocessor [Dobberpuhl92] and many other high performance processors.

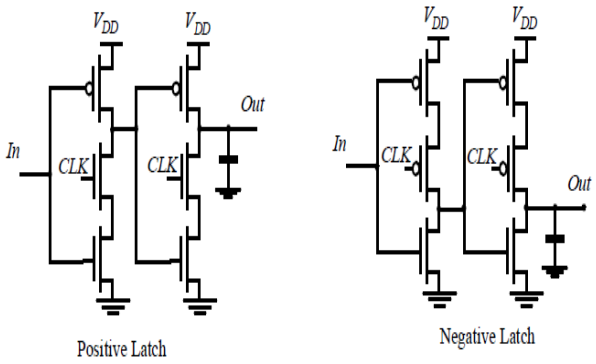


Figure [2].True Single Phase Latches

Consider embedding an AND gate into the TSPC latch, as shown in Figure [3]. In a 0.25µm, the set-up time of such a circuit using minimum-size devices is 140 psec. A conventional approach, composed of an AND gate followed by a positive latch has an effective set-up time of 600 psec (we treat the AND plus latch as a black box that performs the AND latching

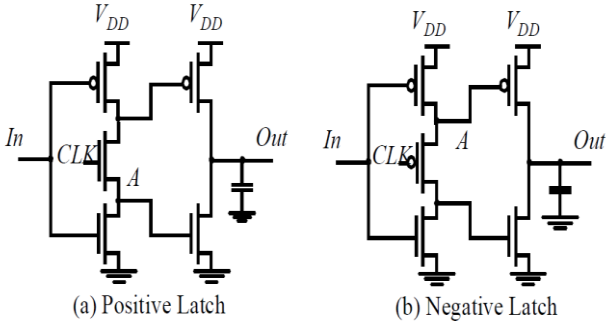


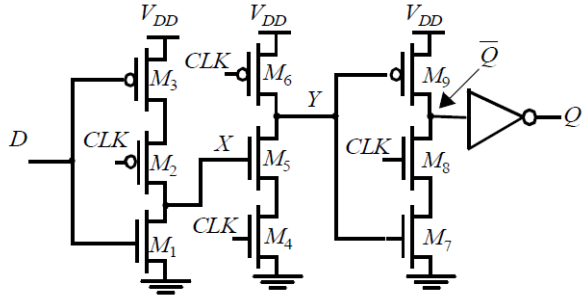
Figure [3]. Simplified TSPC latch

The TSPC latch circuits can be further reduced in complexity as illustrated in Figure [3], where only the first inverter is controlled by the clock. Besides the reduced number of transistors, these circuits have the advantage that the clock load is reduced by half. On the other hand, not all node voltages in the latch experience the full logic swing. For instance, the voltage at node A (for Vin = 0 V) for the positive latch maximally equals VDD– VTn, which results in a reduced drive for the output NMOS transistor and a loss in performance. Similarly, the voltage on node A (for Vin= VDD) for the negative latch is only driven down to |VTp|. This also limits the amount of VDD scaling possible on the latch. Figure [4] shows the design of a specialized single-phase edge-triggered register. When CLK = 0, the input inverter is sampling the inverted D input on node X. The second (dynamic) inverter is in the recharge mode, withM6 charging up node Y to VDD. The third inverter is in the hold mode, since M8 and M9 are off. Therefore, during the low phase of the clock, the input to the final (static) inverter is holding its previous value and the output Q is stable. On the rising edge of the clock, the dynamic inverter M4-M6 evaluates. If X is high on the rising edge, node Y discharges. The third inverter M7-M8 is on during the high phase and the node value on Y is passed to the output Q. On the positive phase of the clock, note that node X transitions to a low if the D input transitions to a high level. Therefore, the input must be

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 10, October 2014

kept stable till the value on node X before the rising edge of the clock propagates to Y. This represents the hold time of the register (note that the hold timeless than 1 inverter delay since it takes 1 delay for the input to affect node X). The propagation delay of the register is essentially three inverters since the value on node X must propagate to the output Q. Finally, the set-up time is the time for node X to be valid, which is one inverter delay.



Figure[4]. Positive edge-triggered register TSPC.

IV. PROPOSED SYSTEM

The E-TSPC 2/3 pre scaler consumes large short circuit power and has a higher frequency of operation than that of TSPC 2/3 pre scaler. The wideband single-phase clock 2/3 pre scaler used in this design consists of two D-flip-flops and two NOR gates embedded in the flip- flops as in Figure [5]. The first NOR gate is embedded in the last stage of first flip flop and second nor gate is embedded in the first stage of second flip flop.

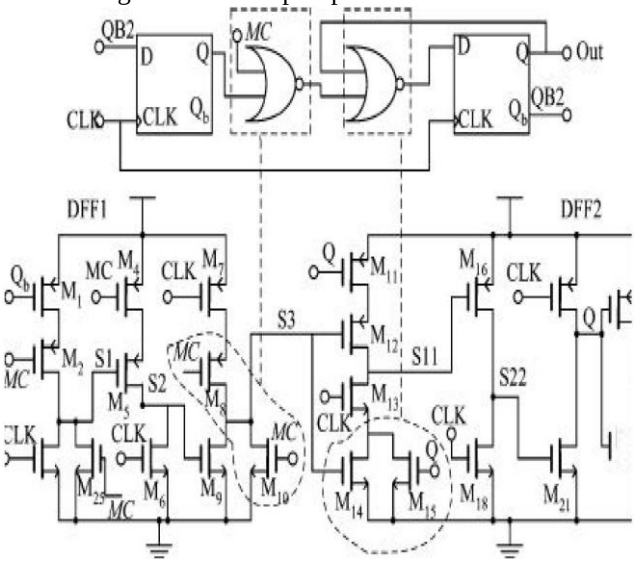


Figure [5].Wideband single phase clock 2/3 prescaler

Here, the transistors M2, M25,M4,Ms in DFFI helps to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal MC. The load capacitance of the prescaler is given by

$$C_{L\text{-}wideband}=C_{dbM19}+2C_{gdM19}+C_{dbM21}+$$

When MC switches from "0" to "I," transistors M2,M4and Ms in DFF 1 turns off and nodes S I, S2 and S3switch to logic "0." Since node S3 is "0" and the other input to the NOR gate embedded in DFF2 is Qb, the wideband pre scaler operates at the divide-by-2 mode. During this mode, nodes S I, S2 and S3 switch to logic"0" and remain at "0" for the entire divide-by-2operation, thus removing the switching power contribution of DFFI. Since one of the transistors is always OFF in each stage of DFFI, the short-circuit power in DFFI and the first stage of DFF2 is negligible. The total power consumption of the pre-scaler in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and third stages of DFF2 and is given b

P widebanb-divide-by-2=l:(,lkCliV$^2_{dd}$+ PSC]+PSC2 (4.2)

Where Cli is the load capacitance at the output node of the ith stage of DFF2, and PSCI and PSC2 are the short circuit power in the second and third stages of DFF2.When logic signal MC switches from "I "to "0," the logic value at the input of DFFI is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFFI is "0" and the wideband prescaler operates at the divide-by-3 mode. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFFI. Thus, the wideband 2/3 pre scaler has benefit of saving more than 50% of power during thedivide-by-2 operation. The measured results shows that the wideband 2/3 prescaler has the maximum operating frequency of 6.5GHz.

4.1 MULTTMODULUS 32/33/47/48 PRESCALER:

The proposed wideband multi-modulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Figure [6]. It is similar to the 32/33 prescaler but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions(divide-by-47 and divide-by-48) without any extra flip flop, thus saving a considerable amount of power and also reducing the complexity of multi band divider.

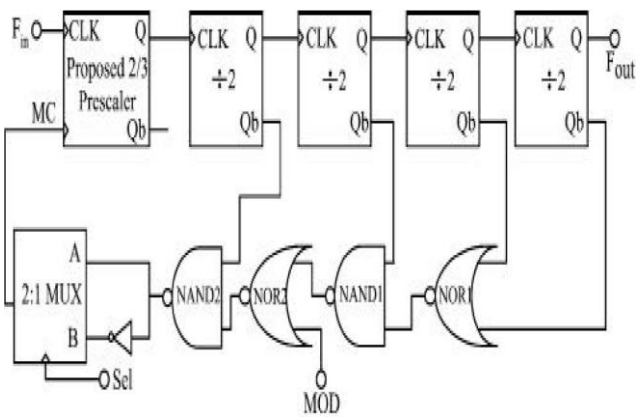


Figure [6] Multi-modulus Prescaler

The multi-modulus prescaler consists of the wideband2/3 (N/(N]+I)) prescaler, four asynchronous TSPCdivide-by-2 circuits ((AD)=16) and combinational logic-circuits to achieve multiple division ratios. Beside the-usual MOD signal for controlling N/(N+l) divisions, the additional control signal sel is used to switch the prescaler between

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 10, October 2014

32/33and 47/48 modes.

1) Case 1: sel='O'

When sel='O', the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multi-modulus prescaler operates as the normal 32/33prescaler, where the division ratio is controlled by the logic signal MOD. If MC=I, the 2/3 prescaler operates in the divide-by-2 mode and when MC=O, the 2/3prescaler operates in the divide-by-3 mode. If MOD=I,the NAND2 gate output switches to logic "I" (MC=I)and the wideband prescaler operates in the divide-by-2mode for entire operation. The division ratio N performed by the multi modulus prescaler is

$$N=(AD*N1)+(O*(N1+ 1))=32 \quad (4.1.1)$$

Where N]=2 and AD=16 is fixed for the entire design. If MOD=O , for 30 input clock cycles MC remains at logic"1", where wideband prescaler operates in divide-by-2mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in theDivide-by-3 mode. The division ratio N+ 1 performed by the multi modulus prescaler is

$$N+l=((AD-l)*N1) \quad (4.1.2)$$

and

S2 switch to logic "0" and the bit-cell does not perform any function. The MOD signal goes logically high only when the S-counter finishes counting down to zero. If MOD and LD are logically low, the bit-cell acts as adivide-by-2 unit. If MOD is logically low and LD islogically high, the input bit PI is transferred to the output. In the initial state, MOD=O, the multi-modulus prescaler selects the divide-by-N+ 1 mode (divide-by-33 or

2) Case 2:sel =' l'

When sel=' 1', the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multi-modulus prescalar operate as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC= 1, the 2/3 prescaler operates individe-by-3 mode and when MC=O, the 2/3 prescaler operatesindivide-by-2 mode which is quite opposite to the operation performed when sel='O' If MOD=I, the division ratio N+ 1 performed by the multi-modulus prescaler is same except that the wideband prescaler operates in the divide by-3 mode for the entire operation given by

$$N+l=(AD*(N1+1))+(0*Nl)=48 \quad (4.1.3)$$

If MOD=I, the division ratio N performed by the multi-modulus prescaler is

$$N=((AD-l)*(N1+1))+(1 *Nl)=47 \quad (4.1.4)$$

4.2 MULTIBAND FLEXBLE DIVIDER:

The single-phase clock multiband flexible divider which is shown in Fig 1.1 consists of the multi modulus32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6 bit swallow S-counter. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5-5.825GHz).

A. Swallow (S) Counter

The 6-bit s-counter shown in Fig.[7]. .consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit cell used in this design shown in Figure [7] is similar to the bit-cell except it uses two additional transistors M6 and M7whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S 1divide-by-48) and P, S counters start down counting the input clock cycles.

When the S-counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-n mode (divide-by-32 ordivide-47) for the remaining P-S clock cycles. During this mode, since S-counter is idle, transistors M6 and M7which are controlled by MOD, keep the nodes S 1 andS2 at logic "0," thus saving the switching power in S counter for a period of (N*(P-S)) clock cycles. Here, the programmable input (PI) is used to load the counter to a specified value from 0 to 31 for the lower band and 0 to 48 for the higher band of operation.

B. Programmable (P) Counter

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P 4 and P7are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=O) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33 (N/(N+ 1)) dual-modulus prescaler is used, a 7bit P counter is needed for the low-frequency band (2.4 GHz)while an 8-bit S-counter would be needed for the high frequency band(5-5.825 GHz) with a fixed 5-bit S counter. Thus, the multimodulus32/33/47/48 prescaler eases the design complexity of the P-counter.

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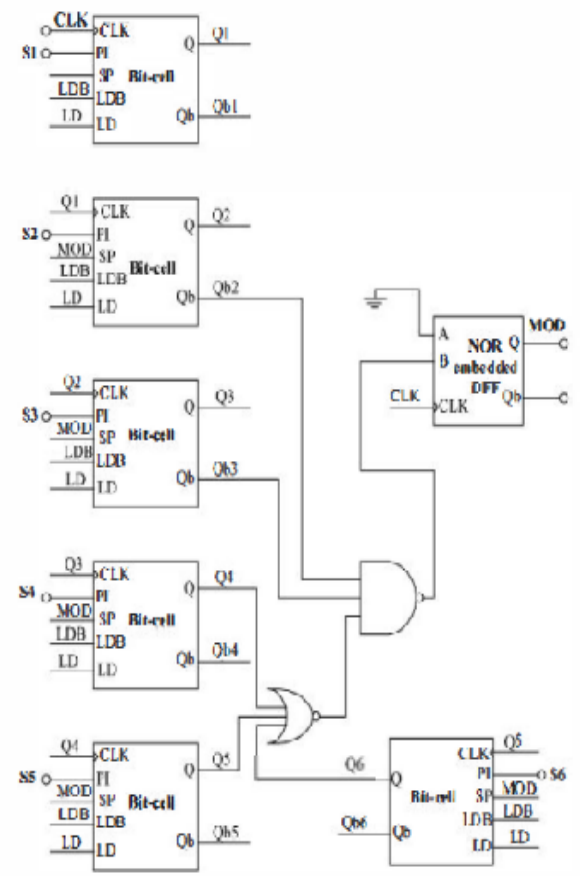

Figure [7].Asynchronous 6-Bit S-Counter

V. RESULT AND DISCUSSION

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	1026	19200	5%
Number of Slice LUTs	3562	19200	18%
Number of fully used LUT-FF pairs	1023	3565	28%
Number of bonded IOBs	2085	220	947%
Number of BUFG/BUFGCTRLs	1	32	3%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Fri Aug 8 11:33:15 2014	0	2 Warnings	0
Translation Report					
Map Report					
Place and Route Report					
Static Timing Report					
Bitgen Report					

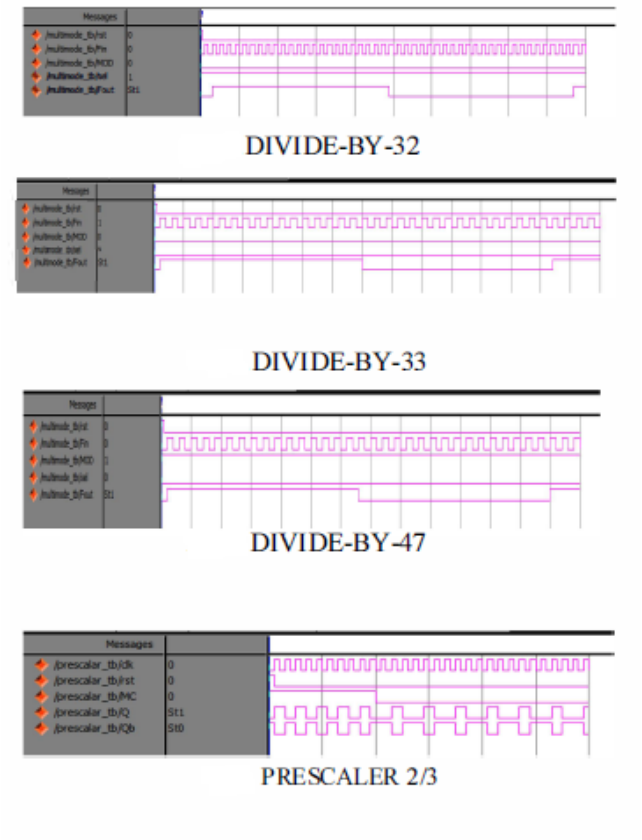

Figure [8] SIMULATED ENVIRONMENT

VI. CONCLUSION

In this paper a simple approach for the low power single phase clock distribution for wireless local area Networks frequency synthesizer is presented. The technique for low power fully programmable divider using design of reload able bit cells for P and S Counter is given. P and S counters can be programmed accordingly for the required bands of frequencies.

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